14.6 A GSM Baseband Radio in 0.13µm CMOS with Fully Integrated Power-Management

Markus Hammes [1], Christian Kranz [1], Jens Kissing [1], Dietolf Seippel[1], Pierre-Henri Bonnaud [2], Enrico Pelos [2]

[1]Infineon Technologies, Duisburg, Germany
[2]Infineon Technologies, Sophia-Antipolis, France

The recent past shows tremendous progress in the area of SoC technology, like fully-integrated GSM/GPRS baseband-radios in standard digital CMOS technology, which represent the key component of a mobile phone. After successfully tackling the challenges of RF integration into a digital baseband chip [1], the next step following the SoC path is the integration of the Power-Management Unit (PMU). To achieve optimum cost, an overall system architecture approach has to be selected that considers the chip-architecture as well as the mobile phone architecture. The integrated PMU not only supplies the functional blocks on-chip but also delivers power to the other components connected to the chip, e.g. LED display lighting, memory and SIM-card. To further decrease the bill-of-materials for the phone the required RAM memory is integrated on-chip, with the FLASH memory connected externally. A typical application example is shown in Fig. 14.6.1.

The chip presented here is derived from the architecture in [1], but, with fundamental extensions, including an integrated PMU (including loudspeaker driver) and fully-integrated RAM. The design faces three major challenges [2,3]: i) the realization of efficient voltage regulators in a digital CMOS technology, ii) electrical and thermal cross-coupling from the regulator and DC/DC-converters to sensitive RF- and audio-circuits, and iii) thermal stress of the CMOS technology.

To achieve the direct-to-battery capability for the regulator and the charger, special circuits are used. In addition other functional blocks, which are typically located in a separate PMU device, have to be integrated, such as a loudspeaker driver with high output power or a DC/DC converter to generate higher voltages than the battery voltage. This higher voltage can be used to supply white or blue LED's.

The selection of the power supply concept, from either linear or switched regulator types, is in general a trade-off between current consumption and cost. A linear regulator results in higher current consumption due to its lower efficiency. Switched regulators, on the other hand, result in higher cost, e.g., if external inductors or if special technology is required as in the case of direct-to-battery connection. The present architecture makes use of both types of regulators. Due to the performance requirements of an ultra-low cost phone, the chip current consumption has been reduced and therefore the majority of the regulators were chosen to be of the linear type.

One major challenge is the high battery voltage (up to 5.5V) compared to the breakdown voltage of the 0.13µm CMOS technology used. This technology provides dual gate oxide transistors (I/O and analog devices) with a drain-source voltage of up to 3.3V. A further increase of the electrical strength requires special design techniques and was achieved by transistor stacking. Theoretically two stacked devices can withstand 6.6V, which is sufficient for the targeted application.

Figure 14.6.2 shows the block diagram of a stacked device direct-to-battery Low-Drop-Out (LDO) regulator. In order to generate an internal reference voltage for the bias circuits and error amplifier the battery voltage is divided by approximately two by means of the serial connection of resistors R3, R4. This voltage is also used (buffered and slightly level-shifted) to drive the second transistor of the pass device in a cascode-like manner. By using a resistor divider feedback network, the error amplifier A1 drives transistor T1 to regulate the output voltage to the target level. The error amplifier design is done like in classical LDO's [2,3].

Figure 14.6.3 presents a summary of the performance parameters achieved with the direct-to-battery design.

Currently the most popular types of battery for mobile phones are lithium ion (Li-Ion) or lithium polymer (Li-Poly) batteries. Nevertheless, for low-cost applications nickel metal hydride (NiMH) or even nickel-cadmium (NiCd) batteries are being used. Therefore the PMU and battery charger has to support all four types of batteries; single cell Li-Ion/Li-Poly and three cell NiMH/NiCd devices. In addition the charger needs to handle peak voltages as high as 30V. These requirements were achieved with the architecture by using only a few low cost external parts. They are required for protecting the PMU against the high charger voltage. Charger-unit types can be 50Hz/60Hz half- or full-wave chargers or switching electronic chargers.

The challenge of limiting the electrical cross-coupling must be met in the design and layout of the chip. It is fundamental to separate the noisy grounds of the DC/DC-converters from sensitive RF and audio grounds. Furthermore noisy blocks have to be separated from sensitive blocks in the layout. Figure 14.6.4 shows a die photo with details of the SoC. The PMU is integrated between the RF, audio and digital macro. This is needed to realize short supply lines. The sensitive RF circuits like the LNA, transmitter and VCO are placed at the opposite side from the PMU inside the RF macro. Figure 14.6.5 shows the TX GSM spectrum at an offset of 400kHz and is one indication that the cross-coupling is well suppressed. The receiver sensitivity in a typical GSM application, including the matching network, is measured as -111dBm (Class II RBER, without fading).

A further challenge is to meet thermal effects due to heating of the PMU. Figure 14.6.6 shows a typical heating profile during burst-mode operation. The complete RF and audio section is affected by the heating of the PMU which cannot be avoided. Therefore, a design issue for sensitive circuits is that they need to be more robust against thermal effects. One sensitive circuit is the RF-PLL. Due to heating, the VCO frequency changes and the operating point of the complete RF-PLL follows the temperature profile. This can lead to a drift in frequency error of the RF-PLL. During transmit burst the GSM performance can be severely degraded by these temperature variations. Figure 14.6.7 shows the frequency error of the transmitter measured in burst mode and proves that the frequency error is well below the GSM limit of 0.1ppm.

For the presented chip a BGA flip-chip package was chosen where the layout is optimized with regard to power routing, analog performance, thermal effects and cross-coupling effects. Despite the additional PMU integration even better performance results have been achieved for the RF as compared to a baseband-radio without integrated PMU [4].

The baseband-radio with integrated PMU is the result of an overall system architecture optimization for an ultra-low cost mobile phone application. This required a consideration of the trade-offs between technology, mobile phone system-architecture, direct-to-battery circuitry and innovative integration concepts. Full GSM/GPRS compliance, including worst-case parameters under extreme operating conditions, is achieved.

Acknowledgments:
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References:
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[3] V. Gupta, G.A. Rincon-Mora, and P. Raha, "Analysis and Design of Monolithic, High PSR, Linear Regulators for SoC Applications," *IEEE SOC Conference*, pp. 311-315, Sept., 2004.
[4] D. Seippel, et al., "GSM/GPRS Single-Chip in 130nm CMOS: Challenges on RF for SoC Integration," *RFIC 2006*, pp. 203-206, June, 2006.

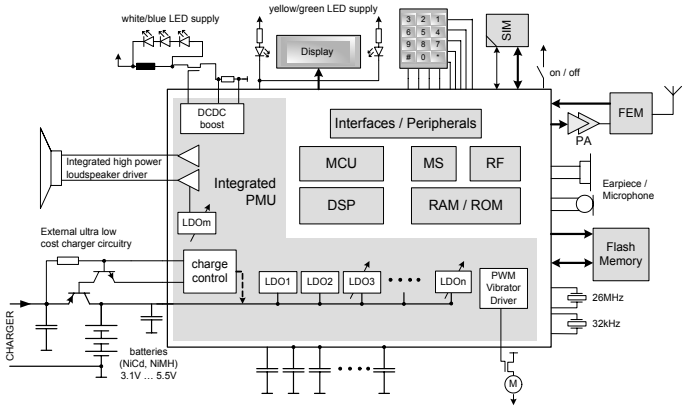

Figure 14.6.1: Block diagram of baseband-radio with integrated PMU.

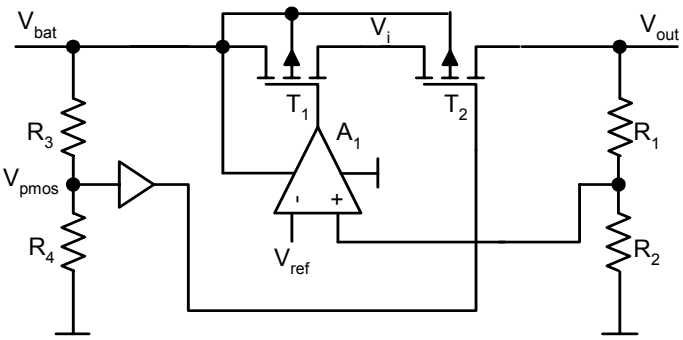

Figure 14.6.2: Schematic for direct-to-battery LDO.

	1.5V LDO	2.5V LDO	Condition
Output current	120mA	100mA	Minimum current
Quiescent current	37µA	39µA	No load current
Line regulation	1mV	1.5mV	Input voltage change 3.1V to 5.5V
Load regulation	10mV	8mV	Load current 1mA to max. LDO current
Line transient response	3mV	2mV	Input voltage 3.1V to 5.5V
Load transient response	14mV	20mV	Load change from 1 to 100mA, Vbat = 3.1V
Power Supply Rejection	67dB	62dB	Frequency range 1 to 20kHz
Chip area	0.18mm^2	0.15mm^2	

Figure 14.6.3: Performance summary of two direct-to-battery LDO's.

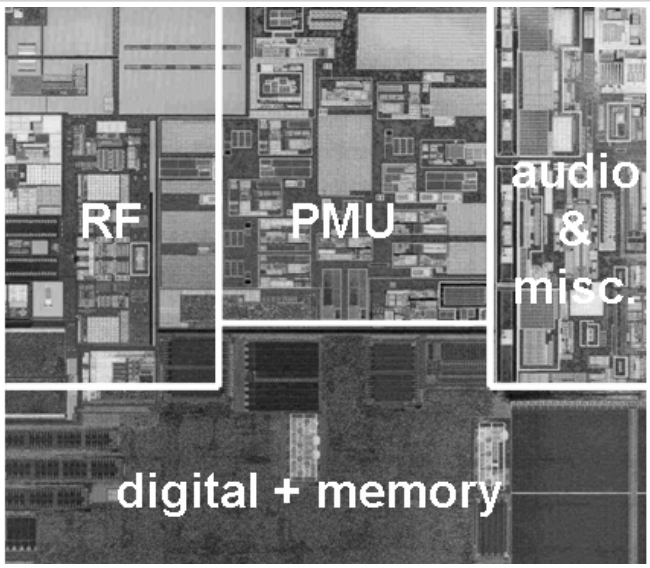

Figure 14.6.4: Chip micrograph of PMU and surrounding sections.

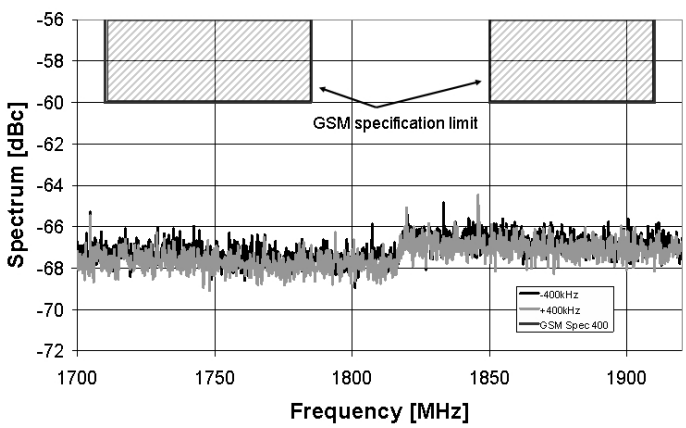

Figure 14.6.5: Measured PRBS modulated TX output power @ +/-400 kHz offset to carrier.

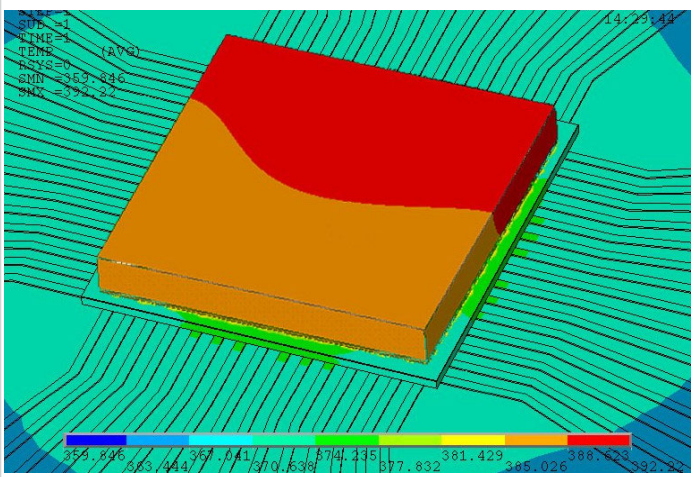

Figure 14.6.6: Thermal heating due to on-chip power dissipation.

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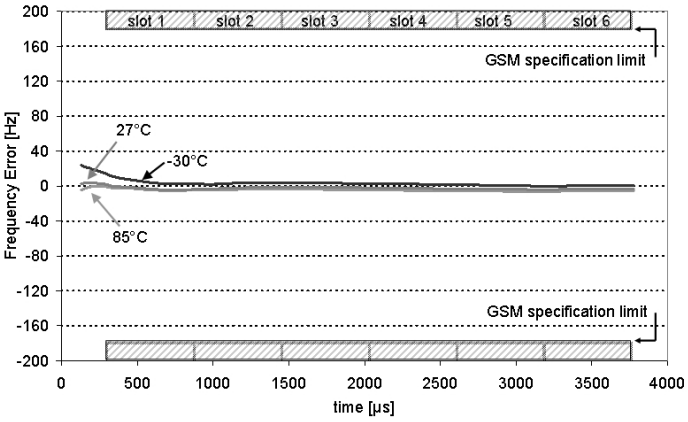

Figure 14.6.7: Frequency error measured in burst mode for different ambient temperatures (including thermal stress caused by PMU).

